

# 8K-bit TTL bipolar PROM (2024x4)

# 82S185/185A/185B

## FEATURES

- Address access time: 55ns max
- Input loading: -150µA max
- On-chip address decoding
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible
- One chip enable input
- Outputs: 3-State

## APPLICATIONS

- Sequential controllers
- Control store
- Random logic
- Code conversion

## DESCRIPTION

The 82S185 is field-programmable, which means that custom patterns are immediately available by following the Philips Generic I fusing procedure. The standard 82S185 is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and one chip enable input for memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

## ORDERING INFORMATION

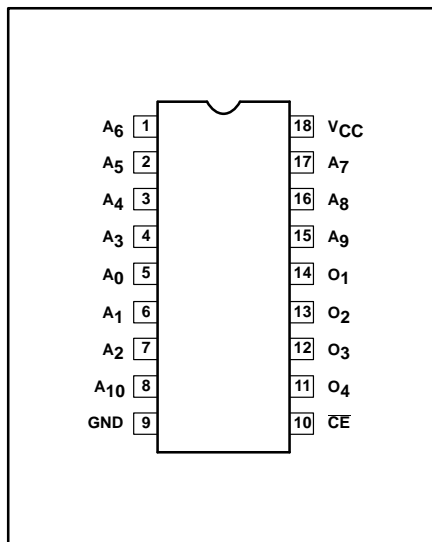
DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
18-pin Ceramic DIP (300mil-wide)	82S185/BVA 82S185A/BVA 82S185B/BVA	GDIP1-T18
18-pin Ceramic Flat Pack	82S185/BYA 82S185A/BYA 82S185B/BYA	GDFF2-F18

\* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

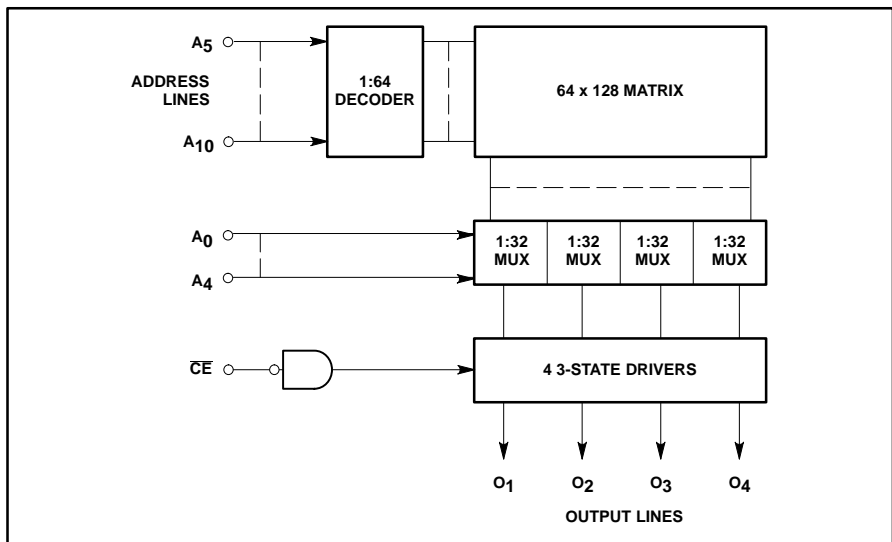
## ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V <sub>CC</sub>	Supply voltage	+7	V <sub>DC</sub>
V <sub>I</sub>	Input voltage	+5.5	V <sub>DC</sub>
V <sub>O</sub>	Output voltage Off-State	+5.5	V <sub>DC</sub>
T <sub>A</sub>	Operating temperature range	-55 to +125	°C
T <sub>STG</sub>	Storage temperature range	-65 to +150	°C

## PIN CONFIGURATION



## BLOCK DIAGRAM



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**DC ELECTRICAL CHARACTERISTICS**  $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ ,  $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1, 2</sup>	LIMITS			UNIT					
			Min	Typ <sup>5</sup>	Max						
<b>Input voltage</b>											
V <sub>IL</sub>	Low	V <sub>CC</sub> = 4.5V, I <sub>I</sub> = -18mA	2.0		0.8	V					
V <sub>IH</sub>	High										
V <sub>IK</sub>	Clamp						-0.8	-1.2	V		
<b>Output voltage</b>											
V <sub>OL</sub>	Low	V <sub>CC</sub> = 4.5V, $\overline{\text{CE}}$ = Low I <sub>O</sub> = 16mA	2.4		0.5	V					
V <sub>OH</sub>	High						I <sub>O</sub> = -2mA	V			
<b>Input current</b>											
I <sub>IL</sub>	Low	V <sub>CC</sub> = 5.5V V <sub>I</sub> = 0.45V			-150	μA					
I <sub>IH</sub>	High						V <sub>I</sub> = 5.5V	40	μA		
<b>Output current</b>											
I <sub>OZ</sub>	Hi-Z state	V <sub>CC</sub> = 5.5V $\overline{\text{CE}}$ = High, V <sub>O</sub> = 0.4V $\overline{\text{CE}}$ = High, V <sub>O</sub> = 5.5V			-40	μA					
I <sub>OS</sub>	Short circuit <sup>3</sup>						$\overline{\text{CE}}$ = Low, V <sub>O</sub> = 0V, High stored	-15		40	μA
<b>Supply current</b>											
I <sub>CC</sub>		$\overline{\text{CE}}$ = High, V <sub>CC</sub> = 5.5V			90	130	mA				
<b>Capacitance<sup>6</sup></b>											
C <sub>IN</sub>	Input	$\overline{\text{CE}}$ = High, V <sub>CC</sub> = 5.0V V <sub>I</sub> = 2.0V			5	10	pF				
C <sub>OUT</sub>	Output							V <sub>O</sub> = 2.0V	8	13	pF

**AC ELECTRICAL CHARACTERISTICS**  $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ ,  $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT	
				Min	Typ <sup>5</sup>	Max		
t <sub>AA</sub>	Access time <sup>4</sup>	185	Output	Address		70	115	ns
		185A			25	55	ns	
		185B			40	90	ns	
t <sub>CE</sub>	Access time <sup>4</sup>	185/185B	Output	Chip Enable		30	50	ns
		185A			15	30	ns	
t <sub>CD</sub>	Disable time	185/185B	Output	Chip Disable		30	50	ns
		185A			15	30	ns	

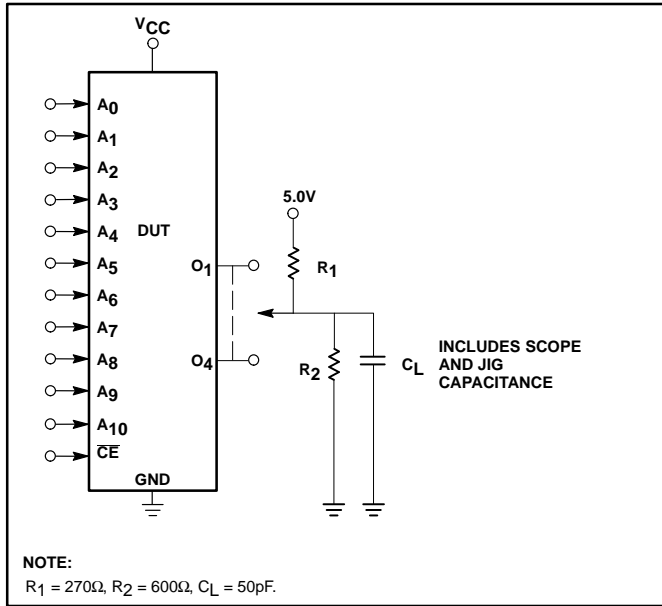
**NOTES:**

1. All voltages are with respect to network ground terminal.
2. Positive current is defined as into the terminal referenced.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at V<sub>CC</sub> = 5V, T<sub>A</sub> = +25°C.
6. Guaranteed, but not tested.

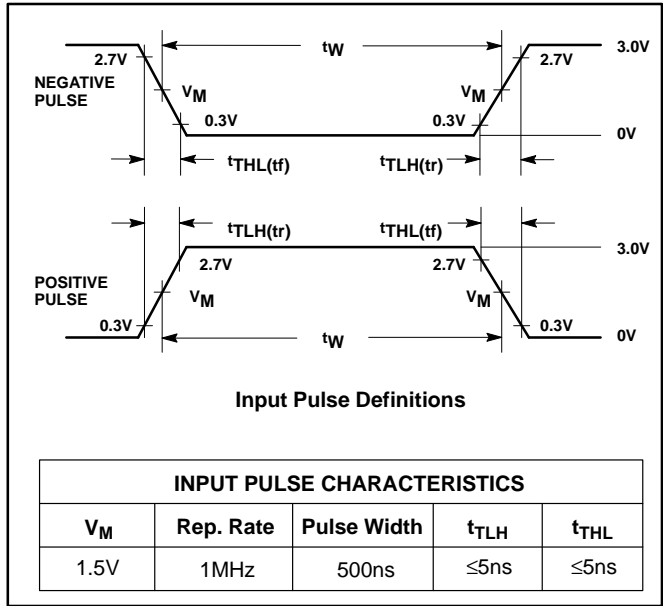
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## TEST LOAD CIRCUITS



## VOLTAGE WAVEFORMS



## TIMING DIAGRAMS

